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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,150	02/13/2004	Woo-jong Park	Q79322	4042
23373 7590 11/07/2008 SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037				
EXAMINER				
AHMED, SALMAN				
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2419				
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/777,150

**Applicant(s)**

PARK, WOO-JONG

**Examiner**

SALMAN AHMED

**Art Unit**

2419

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 7/31/2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 13 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
- Paper No(s)/Mail Date \_\_\_\_\_

- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

**DETAILED ACTION**

Claims 1-12 are pending.

Claims 1-12 are rejected.

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-12 are rejected under 35 U.S.C. 102(e) as being anticipated by Epps et al. (US6977930), hereinafter Epps.

Regarding claim 1, Epps et al. disclose pipelined packet switching and queuing architecture (see column 3 line 10-19) comprising: an input unit for inputting first data in first units of transmission (see figure 2 box 210); a packet memory management unit for assembling the first data into an Internet Protocol (IP) packet and loading the IP packet into a packet memory, and reading out a pointer of an IP packet header and a pointer of an IP packet trailer connected to the IP packet header (see column 5 line 39 -47); • a header processing unit for deciding a packet classification (see column 6 line 24-28 and figure 5 box 520 classifier); and a transmission destination by using the IP packet header, and re-transmitting to the packet memory management unit the pointer of the IP

packet trailer connected to the IP packet header (see column 15 line 12-27); and • an output unit for dividing the IP packet trailer into second data in second units of transmission, the IP packet trailer being read from the packet memory management unit based on the pointer of the IP packet header (see column 9 line 40-45 and column 15 line 67- column 16 line 2 where first tail will always correspond to the first header and figure 3 inherently shows that tails are divided into same size as headers) transmitted from the header processing unit and the pointer of the IP packet trailer connected to the IP packet header, and outputting the second data to a channel (see column 27 line 45-53 and 40 line 4-12). Epps further teaches in column 5 lines 29-33, Also note that while the specific discussion herein relates to Internet Protocol version 4 (IPv4), nothing in the present invention is limited to an IPv4-only implementation. The present invention can also be practiced in connection with the forthcoming IP version 6 (IPv6); thus satisfying the limitation of packets being IP packets. Epps teaches in column 5 lines 44-55, Referring to FIG. 3, incoming packets 113 are then separated into a header portion and a tail portion by byte counter 310, a part of receive FIFO 215. Receive FIFO 215 comprises two logically distinct FIFOs. Header portions, here simply defined as the first n bytes of the received packet, are placed in header FIFO 320. The balance of the packet, i.e., bytes n+1 through the end of the packet, are placed in tail FIFO 330. Here the term "header portion" refers only to the first n bytes of the packet; it is not synonymous with the packet header defined as part of a packet protocol. The length of the header portion n is selected so that it includes the entire protocol header for the types of packets expected in the device. This satisfies limitations related to an output

unit (Figure 3, units 320 and 330 combined) for dividing the IP packet trailer read from the packet memory management unit (Figure 3, Byte counter 310) into second data (figure 3, data residing in Tail FiFO 330) in second units (figure 3, data residing in Tail FiFO 330) of transmission based on the pointer of the IP packet header (pointer of the IP packet header is met by the cited portion: Header portions, here simply defined as the first n bytes (i.e. header pointer) of the received packet, are placed in header FiFO 320. The balance of the packet, i.e., bytes n+1 (i.e. trailer pointer) through the end of the packet, are placed in tail FiFO 330. Here the term "header portion" refers only to the first n (i.e. header pointer) bytes of the packet; The length of the header portion n is selected so that it includes the entire protocol header for the types of packets expected in the device). Epps further teaches in column 8 lines 43-53, column 10 lines 3-11, column 27 lines 45-50, In one embodiment of the present invention, the header and tail portions are multiplexed together by conventional means (not shown) in order to conserve interconnection pins between receive FiFO 215 and pipelined switch 220. On receipt in pipelined switch 220, header portions proceed into the pipeline while tail portions are sent directly to transfer mux 470. Transfer mux 470, as will be discussed below, also conserves interconnection pins by multiplexing the post-pipeline processed header portions and tail portions for transmission to RBM 240. The fetch stage (FS) 410 (FIG. 5) interfaces with receive FiFO 215, which sends the first n bytes, where n is a programmable value, of a packet (the header portion) to it. The FS receives the packet header and writes it into a PHB. Along with the packet header, receive FiFO 215 sends the packet length and channel number information (in the case of linecards having

multiple input interfaces 111), which are stored in packet information register 530. Receive FIFO 215 also sets a flag bit indicating if this header has a corresponding tail portion. FIG. 14 shows an overview of the RBM queue manager 1210. Link manager 1430 is the core of the queue manager. It processes the primitive queuing operations of enqueue and dequeue. It manages the Head and Tail pointers, as well as the per queue-element storage kept in the external queue pointer memory 1215, in some embodiments a SSRAM.

Regarding claim 2, Epps et al. teach the packet memory management unit includes: a packet generator for generating the IP packet from the first data (see column 6 line 17-22 and figure 4 box 410); the packet memory (see figure 12 box 1210 queue manager and column 7 line 11-21) comprising plural buffers (see column 7 line 12 buffers) loading the IP packet, and the plural buffers storing buffer attribute information and the pointer of the IP packet trailer connected to the IP packet header (see column 7 line 17-22 pointers to each buffer); • a transmission header queue for loading the pointer of the IP packet header corresponding to a transmission order of the IP packet (see column 9 line 40-45); and • a controller for reading from the packet memory the pointers of the IP packet header and the IP packet trailer connected to the IP packet header, according to the transmission order determined by the transmission header queue (see column 9 line 40-45), and transmitting the pointers of the IP packet trailer and the IP packet trailer to the header processing unit (see column 9 line 38- 51).

Regarding claim 3, Epps et al. teach the controller, if the pointer of the IP packet trailer connected to the IP packet header is re-transmitted from the header processing

unit, reads the IP packet trailer connected to the IP packet header from a buffer corresponding to the pointer of the IP packet trailer, and transmits the IP packet trailer to the output unit (see column 15 line 12-27).

Regarding claim 4, Epps et al. teach the controller verifies whether a different IP packet trailer connected to the IP packet trailer exists by using the buffer attribute information corresponding to the pointer of the IP packet trailer, and, if the different IP packet trailer exists, reading and transmitting the different IP packet trailer to the output unit (see column 15 line 63 - column 16 line 12 and column 40 line 55 - column 41 line 4).

Regarding claim 5, Epps et al. teach the buffer attribute information includes a front pointer of a front buffer connected to a front of the buffer (see column 16 line 44- 67) and a rear pointer of a rear buffer connected to a rear of the buffer, and information on whether a different IP packet trailer connected after the IP packet trailer, exists (see column 15 line 63 - column 16 line 12 and column 40 line 55 - column 41 line 4).

Regarding claim 11, Epps et al. teach the first units of transmission are the same as the second units of transmission (see column 40 line 39-46).

Regarding claims 6-10 and 12, Epps et al. disclose a packet forwarding method and all the limitations as discussed in the rejection of system claims 1-5 and 11 and are therefore apparatus method claims 6-10 and 12 are rejected using the same rationales.

### ***Response to Arguments***

1. Applicant's arguments see page 7 of the Remarks section, filed 7/31/2008, with respect to the 35 USC 112 rejections of the claims have been fully considered and are persuasive. The 35 USC 112 rejections of the claims have been withdrawn.
2. Applicant's arguments see pages 7-9 of the Remarks section, filed 7/31/2008, with respect to the rejections of the claims have been fully considered and are not persuasive.
3. Applicant argues (see page 8) that the Examiner cites column 9, line 40-45 of Epps as allegedly disclosing an output unit for dividing the IP packet trailer read from the packet memory management unit into second data in second units of transmission based on the pointer of the IP packet header; the cited section, however, merely discloses packet header buffers (PHBs), and do not mention dividing the IP packet trailer read from the packet memory management unit.

However, Examiner respectfully disagrees with the Applicant's assertion. Epps does indeed teach the cited limitations. Specifically, Epps further teaches in column 5 lines 29-33, Also note that while the specific discussion herein relates to Internet Protocol version 4 (IPv4), nothing in the present invention is limited to an IPv4-only implementation. The present invention can also be practiced in connection with the forthcoming IP version 6 (IPv6); thus satisfying the limitation of packets being IP packets. Epps teaches in column 5 lines 44-55, Referring to FIG. 3, incoming packets 113 are then separated into a header portion and a tail portion by byte counter 310, a part of receive FIFO 215. Receive FIFO 215 comprises two logically distinct FIFOs. Header portions, here simply defined as the first n bytes of the received packet, are



placed in header FIFO 320. The balance of the packet, i.e., bytes n+1 through the end of the packet, are placed in tail FIFO 330. Here the term "header portion" refers only to the first n bytes of the packet; it is not synonymous with the packet header defined as part of a packet protocol. The length of the header portion n is selected so that it includes the entire protocol header for the types of packets expected in the device. This satisfies limitations related to an output unit (Figure 3, units 320 and 330 combined) for dividing the IP packet trailer read from the packet memory management unit (Figure 3, Byte counter 310) into second data (figure 3, data residing in Tail FIFO 330) in second units (figure 3, data residing in Tail FIFO 330) of transmission based on the pointer of the IP packet header (pointer of the IP packet header is met by the cited portion: Header portions, here simply defined as the first n bytes (i.e. header pointer) of the received packet, are placed in header FIFO 320. The balance of the packet, i.e., bytes n+1 through the end of the packet, are placed in tail FIFO 330. Here the term "header portion" refers only to the first n (i.e. header pointer) bytes of the packet; The length of the header portion n is selected so that it includes the entire protocol header for the types of packets expected in the device). Examiner further adds that Examiner has cited particular columns, line numbers and/or paragraphs in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in

entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

Applicant argues (see page 8) that In the sections cited by the Examiner, there is no mention of the RBM 1210 or the FIM 170 performing any function which would correspond to "the IP packet trailer being read from the packet memory management unit based on the pointer of the IP packet header transmitted from the header processing unit and the reported pointer of the IP packet trailer to be connected to the IP packet header, and outputting the second data to a channel," as recited in claim 1.

Again, Examiner respectfully disagrees with the Applicant's assertion. As shown above Epps further teaches in column 5 lines 29-33, Also note that while the specific discussion herein relates to Internet Protocol version 4 (IPv4), nothing in the present invention is limited to an IPv4-only implementation. The present invention can also be practiced in connection with the forthcoming IP version 6 (IPv6); thus satisfying the limitation of packets being IP packets. Epps teaches in column 5 lines 44-55, Referring to FIG. 3, incoming packets 113 are then separated into a header portion and a tail portion by byte counter 310, a part of receive FIFO 215. Receive FIFO 215 comprises two logically distinct FIFOs. Header portions, here simply defined as the first n bytes of the received packet, are placed in header FIFO 320. The balance of the packet, i.e., bytes n+1 through the end of the packet, are placed in tail FIFO 330. Here the term "header portion" refers only to the first n bytes of the packet; it is not synonymous with the packet header defined as part of a packet protocol. The length of the header portion n is selected so that it includes the entire protocol header for the types of packets

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receive FIFO 215 and pipelined switch 220. On receipt in pipelined switch 220, header portions proceed into the pipeline while tail portions are sent directly to transfer mux 470. Transfer mux 470, as will be discussed below, also conserves interconnection pins by multiplexing the post-pipeline processed header portions and tail portions for transmission to RBM 240. The fetch stage (FS) 410 (FIG. 5) interfaces with receive FIFO 215, which sends the first n bytes, where n is a programmable value, of a packet (the header portion) to it. The FS receives the packet header and writes it into a PHB. Along with the packet header, receive FIFO 215 sends the packet length and channel number information (in the case of linecards having multiple input interfaces 111), which are stored in packet information register 530. Receive FIFO 215 also sets a flag bit indicating if this header has a corresponding tail portion. FIG. 14 shows an overview of the RBM queue manager 1210. Link manager 1430 is the core of the queue manager. It processes the primitive queuing operations of enqueue and dequeue. It manages the Head and Tail pointers, as well as the per queue-element storage kept in the external queue pointer memory 1215, in some embodiments a SSRAM. Examiner further adds that Examiner has cited particular columns, line numbers and/or paragraphs in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed

invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

As such claims 1-12 stands rejected.

***Conclusion***

2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **SALMAN AHMED** whose telephone number is (571)272-8307. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edan Orgad can be reached on (571) 272-7884. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/S. A./

Examiner, Art Unit 2419

/Edan Orgad/

Supervisory Patent Examiner, Art Unit 2419